APPENDIX C

(CLEAN VERSION OF ALL PENDING CLAIMS)

(Serial No. 09/960,089)

CLAIMS

What is claimed is:

1. (Amended) A stacked semiconductor assembly, comprising:

a first semiconductor die including an active surface and a backside, said active surface including a plurality of bond pads and at least one redistribution bond pad circuit thereon, said plurality of bond pads electrically connected to integrated circuitry of said first semiconductor die, said at least one redistribution bond pad circuit independent from said integrated circuitry of said first semiconductor die and including a plurality of redistribution bond pads;

a second semiconductor die including an active surface, a backside, and a plurality of bond pads on said active surface thereof, said active surface of said second semiconductor die facing said active surface of said first semiconductor die; and

at least one electrical connector extending between at least one bond pad of said plurality of bond pads on said active surface of said second semiconductor die and at least one redistribution bond pad of said plurality of redistribution bond pads on said first semiconductor die.

2. (Amended) The stacked semiconductor assembly of claim 1, wherein said first semiconductor die is disposed on a substrate.

3. (Amended) The stacked semiconductor assembly of claim 2, wherein said first semiconductor die is electrically connected to said substrate with intermediate conductive elements.

4. (Amended) The stacked semiconductor assembly of claim 3, wherein said intermediate conductive elements comprise bond wires.

5. (Amended) The stacked semiconductor assembly of claim 2, wherein said at least one redistribution bond pad circuit comprises a plurality of conductive traces, at least one conductive trace of said plurality of conductive traces connecting a first redistribution bond pad of said plurality of redistribution bond pads and a second redistribution bond pad of said plurality of redistribution bond pads, said second redistribution bond pad proximate the perimeter of said first semiconductor die.

6. (Amended) The stacked semiconductor assembly of claim 5, wherein said second redistribution bond pad is electrically connected to said substrate.

7. (Amended) The stacked semiconductor assembly of claim 1, wherein peripheral edges of said first semiconductor die and edges of said second semiconductor die are substantially vertically aligned.

8. (Amended) The stacked semiconductor assembly of claim 1, wherein said second semiconductor die is smaller than said first semiconductor die.

9. (Amended) The stacked semiconductor assembly of claim 1, wherein said at least one electrical connector spaces the active surface of said second semiconductor die from the active surface of said first semiconductor die.

10. (Amended) The stacked semiconductor assembly of claim 1, further comprising a substrate under said first semiconductor die, said substrate including a plurality of contact areas thereon.

11. (Amended) The stacked semiconductor assembly of claim 10, wherein at least one bond pad of said plurality of bond pads on said first semiconductor die is electrically connected to a corresponding contact area of said plurality of contact areas on said substrate.

12. (Amended) The stacked semiconductor assembly of claim 10, wherein said at least one redistribution bond pad is electrically connected to a corresponding contact area of said plurality of contact areas on said substrate.

13. (Amended) The stacked semiconductor assembly of claim 10, further comprising at least one semiconductor die vertically stacked on said substrate, wherein said backside of said first semiconductor is located above said at least one stacked semiconductor die.

14. (Amended) The stacked semiconductor assembly of claim 1, further comprising an insulative layer between said first semiconductor die and said second semiconductor die.

15. (Amended) The stacked semiconductor assembly of claim 14, wherein said insulative layer comprises an adhesive material.

16. (Amended) The stacked semiconductor assembly of claim 1, wherein said at least one electrical connector comprises a substantially columnar pillar.

17. (Amended) The stacked semiconductor assembly of claim 16, wherein said substantially columnar pillar is copper.

18. (Amended) The stacked semiconductor assembly of claim 1, wherein said at least one electrical connector comprises a solder ball.

19. (Amended) The stacked semiconductor assembly of claim 1, wherein at least one peripheral edge of said second semiconductor die extends laterally beyond at least one corresponding peripheral edge of said first semiconductor die.

20. (Amended) The stacked semiconductor assembly of claim 19, further comprising at least one electrical connector extending from at least one bond pad of said plurality of bond pads on said second semiconductor die and a corresponding contact area of a substrate.

21. (Amended) The stacked semiconductor assembly of claim 1, wherein at least one peripheral edge of said first semiconductor die extends laterally beyond at least one corresponding peripheral edge of said second semiconductor die.

22. (Amended) A semiconductor assembly, comprising:

a substrate;

a first semiconductor die including an active surface, a second surface, and a plurality of peripheral edges, said second surface disposed on said substrate, said active surface having a plurality of bond pads thereon;

a second semiconductor die including an active surface, a second surface, a plurality of peripheral edges and a plurality of bond pads on said active surface, said active surface of said second semiconductor die facing said active surface of said first semiconductor die, at least one edge of said plurality of peripheral edges of said second semiconductor die extending laterally beyond at least one corresponding peripheral edge of said plurality of peripheral edges of said first semiconductor die; and

at least one connective element extending from at least one bond pad of said plurality of bond pads on said active surface of said second semiconductor die to a corresponding contact area of said substrate adjacent to said at least one corresponding peripheral edge of said first semiconductor die.

23. The semiconductor assembly of claim 22, further comprising at least one additional semiconductor die stacked vertically between said first semiconductor die and said second semiconductor die.

24. (Amended) The semiconductor assembly of claim 23, wherein said at least one additional semiconductor die and said first semiconductor die are all electrically connected to said substrate by discrete conductive elements.

25. (Amended) The semiconductor assembly of claim 23, wherein a third semiconductor die of said at least one additional semiconductor die is disposed directly below said second semiconductor die, said third semiconductor die including an active surface and a backside, said active surface including a plurality of bond pads and at least one redistribution bond pad circuit thereon, said plurality of bond pads of said third semiconductor die electrically connected to integrated circuitry of said third semiconductor die, said at least one redistribution bond pad circuit independent from the integrated circuitry of said third semiconductor die and including a plurality of redistribution bond pads.

26. The semiconductor assembly of claim 25, wherein said at least one redistribution bond pad circuit comprises a plurality of conductive traces, at least one conductive trace of said plurality of conductive traces connecting a first redistribution bond pad of said plurality of redistribution bond pads and a second redistribution bond pad of said plurality of redistribution bond pads, said second redistribution bond pad proximate the perimeter of said third semiconductor die.

27. (Amended) The semiconductor assembly of claim 26, wherein at least one connective element extends between said least one bond pad on said active surface of said second semiconductor die and said first redistribution bond pad on said active surface of said third semiconductor die.

28. The semiconductor assembly of claim 27, wherein said second redistribution bond pad is electrically connected to said substrate by discrete conductive elements.

29. The semiconductor assembly of claim 24, wherein said discrete conductive elements comprise at least one of wire bonds, TAB elements, and leads.

A4 30. (Amended) The semiconductor assembly of claim 22, wherein said at least one connective element comprises a substantially columnar pillar.

31. The semiconductor assembly of claim 30, wherein said substantially columnar pillar is copper.

32. The semiconductor assembly of claim 22, wherein said at least one connective element comprises a solder ball.

33. The semiconductor assembly of claim 22, wherein said at least one connective element extends from said at least one bond pad of said second semiconductor die to said corresponding contact area of said substrate.

34. The semiconductor assembly of claim 22, further comprising an insulative layer between said first semiconductor die and said second semiconductor die.

35. The semiconductor assembly of claim 34, wherein said insulative layer comprises an adhesive material.

36. A method of forming a stacked semiconductor assembly, comprising:

providing a first semiconductor die including an active surface and a backside, said active surface including integrated circuitry, a plurality of bond pads, a plurality of redistribution pads and a plurality of metal traces thereon, said plurality of redistribution pads independent from said integrated circuitry, at least one metal trace of said plurality of metal traces connecting at least a first redistribution pad of said plurality of redistribution pads and at least a second redistribution pad of said plurality of redistribution pads;

providing a second semiconductor die including an active surface and a backside, said active surface of said first semiconductor die facing said active surface of said second semiconductor die, said active surface of said second semiconductor die including a plurality of bond pads thereon;

electrically connecting said first redistribution pad of said first semiconductor die and a corresponding bond pad of said plurality of bond pads of said second semiconductor die; and

electrically connecting said second redistribution pad of said first semiconductor die and a corresponding contact area of a substrate.

37. The method according to claim 36, further comprising disposing said backside of said first semiconductor die on said substrate and electrically connecting at least one bond pad of said plurality of bond pads of said first semiconductor die to a corresponding contact area of said substrate.

38. The method according to claim 36, wherein said electrically connecting said second redistribution pad and said corresponding contact area comprises extending discrete conductive elements between said second redistribution pad and said substrate.

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39. (Amended) The method according to claim 36, further comprising:

providing at least one additional semiconductor die on said substrate; and

disposing said backside of said first semiconductor die on said at least one additional semiconductor die.

40. The method according to claim 36, further comprising providing an insulative layer between said first semiconductor die and said semiconductor second die.

41. (Amended) The method according to claim 36, wherein said electrically connecting said first redistribution pad and said corresponding bond pad comprises extending a conductive element between said corresponding bond pad of said second semiconductor die and said first redistribution pad of said first semiconductor die.

42. The method according to claim 36, wherein said providing said second semiconductor die comprises substantially vertically aligning at least one edge of said second semiconductor die and at least one edge of said first semiconductor die.

43. The method according to claim 36, further comprising encapsulating said stacked semiconductor assembly.

44. The method according to claim 36, wherein said electrically connecting said second redistribution pad and said corresponding contact area comprises extending conductive elements from said second redistribution pad on one side of said substrate through an aperture in said substrate to said corresponding contact area on an opposite side of said substrate.

45. (Amended) A method of forming a stacked semiconductor package, comprising:

providing a substrate including a plurality of contact areas;

providing a first semiconductor die including an active surface, a backside, and a plurality of peripheral edges, said backside surface disposed above said substrate, said active surface including a plurality of bond pads thereon;

disposing a top semiconductor die above said first semiconductor die, said top semiconductor die including an active surface, a backside and a plurality of peripheral edges, said active surface of said top semiconductor die facing said active surface of said first semiconductor die and including a plurality of bond pads thereon, at least one edge of said plurality of peripheral edges of said top semiconductor die extending laterally beyond at least one corresponding peripheral edge of said plurality of peripheral edges of said first semiconductor die; and

extending at least one conductive element between at least one bond pad of said plurality of bond pads on said top semiconductor die and a corresponding contact area of said plurality of contact areas of said substrate adjacent to said at least one corresponding peripheral edge of said first semiconductor die.

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46. The method according to claim 45, further comprising:

stacking at least one additional semiconductor die vertically on said substrate, wherein said backside of said first semiconductor die is disposed on said at least one additional semiconductor die.

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47. (Amended) The method according to claim 45, further comprising electrically connecting at least one bond pad of said plurality of bond pads of said first semiconductor die and a corresponding contact area of said substrate.

48. The method according to claim 45, further comprising forming at least one redistribution bond pad circuit on said active surface of said first semiconductor die, said at least one redistribution bond pad circuit independent from integrated circuitry of said first semiconductor die and including a plurality of redistribution bond pads.

49. The method according to claim 48, wherein said forming comprises electrically connecting a first redistribution bond pad of said plurality of redistribution bond pads and a second redistribution bond pad of said plurality of redistribution bond pads, said second redistribution bond pad proximate the perimeter of said first semiconductor die.

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50. (Amended) The method according to claim 45, wherein said providing said first semiconductor die comprises providing a first semiconductor die including at least one redistribution bond pad circuit on said active surface thereof, said at least one redistribution bond pad circuit independent from integrated circuitry of said first semiconductor die and including a plurality of redistribution bond pads.

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51. (Amended) The method according to claim 50, wherein said providing said first semiconductor die further comprises electrically connecting a first redistribution bond pad of said plurality of redistribution bond pads and a second redistribution bond pad of said plurality of redistribution bond pads, said second redistribution bond pad proximate the perimeter of said first semiconductor die.

52. (Amended) The method according to claim 51, further comprising extending at least one connective element between at least one bond pad of said plurality of bond pads on said active surface of said semiconductor die and said first redistribution bond pad on said active surface of said first semiconductor die.

53. The method according to claim 52, further comprising electrically connecting said second redistribution bond pad and a corresponding contact area of said substrate.

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54. (Amended) The method according to claim 53, wherein said electrically connecting comprises extending at least one discrete conductive element between said second redistribution bond pad and corresponding contact area of said substrate.

55. (Amended) The method according to claim 54, wherein said at least one discrete conductive element comprises at least one of wire bonds, TAB elements, and leads.

56. (Amended) The method according to claim 45, wherein said extending at least one conductive element comprises extending a substantially columnar pillar between said at least one bond pad of said plurality of bond pads on said top semiconductor die and said corresponding contact area of said substrate adjacent said at least one corresponding peripheral edge of said first semiconductor die.

57. (Amended) The method according to claim 45, wherein said extending at least one conductive element comprises extending a solder ball between said at least one bond pad of said plurality of bond pads on said top semiconductor die and said corresponding contact area of said substrate adjacent to said at least one corresponding peripheral edge of said first semiconductor die.

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58. (Amended) The method according to claim 45, wherein said extending said at least one conductive element comprises extending at least one conductive element from said at least one bond pad of said top semiconductor die to said corresponding contact area of said substrate.

59. (Amended) The method according to claim 45, further comprising providing an insulative layer between said first semiconductor die and said top semiconductor die.

60. (Amended) The method according to claim 59, wherein said providing said insulative layer comprises providing a layer of adhesive material.

61. (Amended) The method according to claim 45, further comprising encapsulating said stacked semiconductor package.

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62. A method of designing a semiconductor device to be used as a lower semiconductor device in a stacked semiconductor assembly, said method comprising:

providing a first semiconductor device including an active surface and a backside, said active surface including integrated circuitry and a plurality of bond pads thereon; and

designing at least one redistribution circuit on said active surface, said redistribution circuit independent from said integrated circuitry.

63. The method according to claim 62, wherein said designing said at least one redistribution circuit comprises providing at least one first redistribution bond pad and at least one second redistribution bond pad.

64. The method according to claim 63, wherein said designing said at least one redistribution circuit further comprises electrically connecting said at least one first redistribution bond pad and said at least one second redistribution bond pad.

65. The method according to claim 64, wherein said electrically connecting comprises extending a metal trace between said at least one first redistribution bond pad and said at least one second redistribution bond pad.

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66. (Amended) The method according to claim 63, wherein said providing said at least one first redistribution bond pad comprises providing at least one first redistribution bond pad positioned on said active surface in a location that mirrors a location of a corresponding bond pad of a second semiconductor device to be positioned over said first semiconductor device.

67. (Amended) The method according to claim 63, wherein said designing said at least one redistribution circuit comprises:
forming a first dielectric layer on said active surface;
etching said first dielectric layer;
depositing a metal layer over said first dielectric layer;
etching said metal layer;
forming a second dielectric layer over said metal layer; and
etching said second dielectric layer.

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68. The method according to claim 67, wherein said etching said first dielectric layer exposes said at least one first redistribution bond pad.

69. The method according to claim 67, wherein said etching said metal layer creates a metal trace.

70. The method according to claim 67, wherein said etching said second dielectric layer exposes said at least one second redistribution bond pad.

71. The method according to claim 67, further comprising depositing a passivation layer on said active surface.

72. The method according to claim 71, wherein said passivation layer comprises nitride or silicon nitride.

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73. (Amended) The method according to claim 67, wherein said first dielectric layer comprises polyimide or BCB.

74. The method according to claim 67, wherein said metal layer is selected from the group consisting of titanium, copper, aluminum, NiV and nickel.

75. The method according to claim 67, wherein said depositing said metal layer comprises sputtering.

76. A semiconductor device for use in a stacked semiconductor assembly, said semiconductor device comprising:
a backside;
an active surface including a plurality of bond pads; and
at least one redistribution bond pad circuit on said active surface, said at least one redistribution bond pad circuit independent from integrated circuitry of said semiconductor device.

77. (Amended) The semiconductor device of claim 76, wherein said plurality of bond pads is electrically connected to said integrated circuitry of said semiconductor device.

78. (Amended) The semiconductor device of claim 77, wherein said plurality of bond pads is centrally located on said active surface.

79. (Amended) The semiconductor device of claim 77, wherein said plurality of bond pads is located proximate the perimeter of said active surface.

80. (Amended) The semiconductor device of claim 76, wherein said at least one redistribution bond pad circuit comprises a first redistribution bond pad electrically connected to a second redistribution bond pad.

81. (Amended) The semiconductor device of claim 80, wherein said at least one redistribution bond pad circuit further comprises a conductive trace extending between said first redistribution bond pad and said second redistribution bond pad.

82. The semiconductor device of claim 81, wherein said conductive trace comprises at least one of titanium, copper, aluminum, NiV and nickel.

83. The semiconductor device of claim 80, wherein said first redistribution bond pad is located on said active surface in a location that mirrors a location of a corresponding bond pad of a second semiconductor device to be positioned above said semiconductor device.

84. The semiconductor device of claim 83, wherein said second redistribution bond pad is proximate the perimeter of said semiconductor device.

85. The semiconductor device of claim 80, wherein said first redistribution bond pad is electrically connected to a corresponding bond pad on an active surface of a second semiconductor device.

86. The semiconductor device of claim 85, wherein said second redistribution bond pad is electrically connected to a contact area on a substrate.

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87. (Amended) A method for redistributing bond pads of a semiconductor device, said method comprising:

providing a semiconductor device including an active surface having a first set of substantially centrally located bond pads and a second set of substantially peripherally located bond pads thereon, said second set of substantially peripherally located bond pads and said first set substantially centrally located bond pads electrically independent from said semiconductor device; and

electrically connecting at least one bond pad of said first set of substantially centrally located bond pads to a corresponding second bond pad of said second set of substantially peripherally located bond pads.

88. The method according to claim 87, wherein said electrically connecting comprises extending a metal trace between said at least one bond pad and said corresponding second bond pad.

89. The method according to claim 87, wherein said electrically connecting said at least one bond pad comprises:

forming a first dielectric layer on said active surface;

depositing a metal layer over said first dielectric layer; and

forming a second dielectric layer over said metal layer.

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90. (Amended) The method according to claim 89, further comprising etching said first dielectric layer to expose said at least one bond pad of said first set of substantially centrally located bond pads.

91. (Amended) The method according to claim 89, further comprising etching said metal layer to create a metal trace between said at least one bond pad and said corresponding second bond pad.

92. The method according to claim 89, further comprising etching said second dielectric layer to expose said corresponding second bond pad.

93. The method according to claim 89, further comprising depositing a passivation layer on said active surface.

94. The method according to claim 93, wherein said passivation layer comprises nitride or silicon nitride.

95. The method according to claim 89, wherein said first dielectric layer comprises polyimide or BCB.

96. The method according to claim 89, wherein said metal layer is selected from the group consisting of titanium, copper, aluminum, NiV and nickel.

97. The method according to claim 89, wherein said depositing said metal layer comprises sputtering.